Self-Protected Low Side Driver with In-Rush Current Management

NCV8415

The NCV8415 is a three terminal protected Low−Side Smart Discrete FET. The protection features include Delta Thermal Shutdown, overcurrent, overtemperature, ESD and integrated Drain−to−Gate clamping for overvoltage protection. The device also offers fault indication via the gate pin. This device is suitable for harsh automotive environments.

Features

- Short−Circuit Protection with In−Rush Current Management
- Delta Thermal Shutdown
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Overvoltage Protection and Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

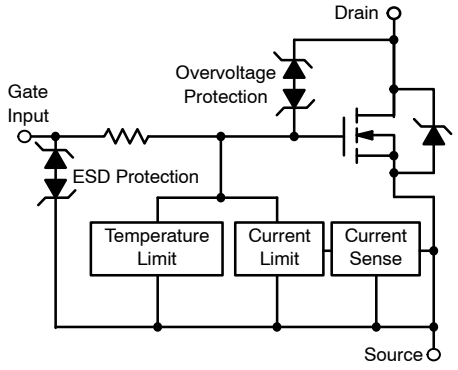

Figure 1. Block Diagram

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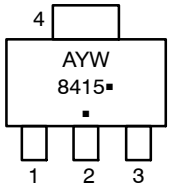
V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
42 V	80 mΩ @ 10 V	11 A

SOT−223
CASE 318E
STYLE 3

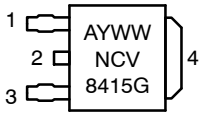
DPAK
CASE 369C
STYLE 2

MARKING DIAGRAMS



SOT−223

Pin Marking Information
1 = Gate
2 = Drain
3 = Source
4 = Drain



DPAK

A = Assembly Location
Y = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV8415DTRKG	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8415STT1G	SOT−223 (Pb−Free)	1000 / Tape & Reel
NCV8415STT3G	SOT−223 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	V
Drain−to−Gate Voltage Internally Clamped	V_{DG}	42	V
Gate−to−Source Voltage	V_{GS}	±14	V
Drain Current − Continuous	I_D	Internally Limited	
Total Power Dissipation (SOT−223) @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2) Total Power Dissipation (DPAK) @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.29 2.20 1.54 2.99	W
Thermal Resistance (SOT−223) Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2) Junction−to−Case (Soldering Point) Thermal Resistance (DPAK) Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2) Junction−to−Case (Soldering Point)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$ $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	 96.4 56.8 10.6 80.8 41.8 3.2	°C/W
Single Pulse Inductive Load Switching Energy (L = 10 mH, I_{Lpeak} = 4.2 A, V_{GS} = 5 V, R_G = 25 Ω, T_{Jstart} = 25°C)	E_{AS}	88	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_L = 10 Ω) (Note 3)	U_S*	52	V
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	$T_{storage}$	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted onto a 80 × 80 × 1.6 mm single layer FR4 board (100 sq mm, 1 oz. Cu, steady state).
2. Mounted onto a 80 × 80 × 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state).
3. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750−1.

ESD ELECTRICAL CHARACTERISTICS (Note 4, 5)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	4000	−	−	V
	Charged Device Model (CDM)		1000	−	−	

4. Not tested in production.
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017).
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 × 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

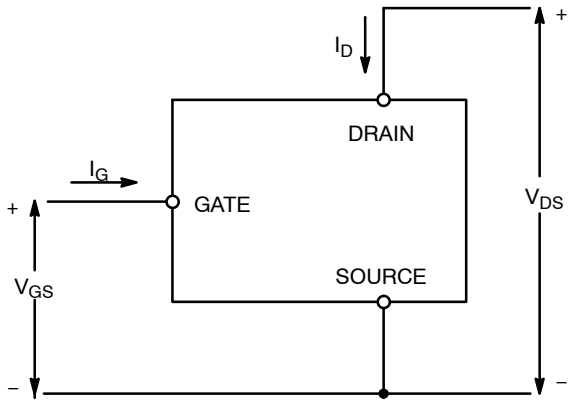


Figure 2. Voltage and Current Convention

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA	$V_{(BR)DSS}$	42	46	51	V
	V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C (Note 6)		42	44	51	
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 32 V	I_{DSS}	–	0.6	2.0	μA
	V_{GS} = 0 V, V_{DS} = 32 V, T_J = 150°C (Note 6)		–	2.4	10	
Gate Input Current	V_{GS} = 5 V, V_{DS} = 0 V	I_{GSS}	–	50	70	
ON CHARACTERISTICS						
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 150 μA	$V_{GS(th)}$	1.0	1.6	2.0	V
Gate Threshold Temperature Coefficient	V_{GS} = V_{DS}, I_D = 150 μA (Note 6)	$V_{GS(th)}/T_J$	–	−4.0	–	mV/°C
Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 1.4 A	$R_{DS(ON)}$	–	80	100	mΩ
	V_{GS} = 10 V, I_D = 1.4 A, T_J = 150°C (Note 6)		–	150	190	
	V_{GS} = 5.0 V, I_D = 1.4 A		–	105	120	
	V_{GS} = 5.0 V, I_D = 1.4 A, T_J = 150°C (Note 6)		–	185	210	
	V_{GS} = 5.0 V, I_D = 0.5 A		–	105	120	
	V_{GS} = 5.0 V, I_D = 0.5 A, T_J = 150°C (Note 6)		–	185	210	
Source−Drain Forward On Voltage	I_S = 7 A, V_{GS} = 0 V	V_{SD}	–	0.88	1.10	V
SWITCHING CHARACTERISTICS (Note 6)						
Turn−On Time (10% V_{GS} to 90% I_D)	V_{GS} = 0 V to 5 V, V_{DD} = 12 V, I_D = 1 A	t_{ON}	–	30	35	μs
Turn−Off Time (90% V_{GS} to 10% I_D)		t_{OFF}	–	44	55	
Turn−On Time (10% V_{GS} to 90% I_D)	V_{GS} = 0 V to 10 V, V_{DD} = 12 V, I_D = 1 A	t_{ON}	–	13	20	
Turn−Off Time (90% V_{GS} to 10% I_D)		t_{OFF}	–	70	90	
Turn−On Rise Time (10% I_D to 90% I_D)		t_{rise}	–	9	15	
Turn−Off Fall Time (90% I_D to 10% I_D)		t_{fall}	–	29	40	
Slew Rate On (80% V_{DS} to 50% V_{DS})		$-dV_{DS}/dt_{ON}$	0.5	1.63	–	V/μs
Slew Rate Off (50% V_{DS} to 80% V_{DS})		dV_{DS}/dt_{OFF}	0.4	0.55	–	
SELF PROTECTION CHARACTERISTICS						
Current Limit	V_{GS} = 5 V, V_{DS} = 10 V	I_{LIM}	7.0	8.8	11	A
	V_{GS} = 5 V, V_{DS} = 10 V, T_J = 150°C (Note 6)		6.4	7.9	9.1	
	V_{GS} = 10 V, V_{DS} = 10 V (Note 6)		5.2	8.2	11	
	V_{GS} = 10 V, V_{DS} = 10 V, T_J = 150°C (Note 6)		5.0	7.4	10	
Temperature Limit (Turn−Off)	V_{GS} = 5.0 V (Note 6)	$T_{LIM(OFF)}$	150	175	185	°C
Thermal Hysteresis		$\Delta T_{LIM(ON)}$	–	15	–	
Temperature Limit (Turn−Off)	V_{GS} = 10 V (Note 6)	$T_{LIM(OFF)}$	150	185	200	
Thermal Hysteresis		$\Delta T_{LIM(ON)}$	–	15	–	
GATE INPUT CHARACTERISTICS (Note 6)						
Device ON Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V, I_D = 1 A	I_{GON}	35	50	70	μA
	V_{GS} = 10 V, V_{DS} = 10 V, I_D = 1 A		250	310	450	
Current Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GCL}	45	76	95	
	V_{GS} = 10 V, V_{DS} = 10 V		320	450	550	
Thermal Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V, I_D = 0 A	I_{GTL}	210	240	260	
	V_{GS} = 10 V, V_{DS} = 10 V, I_D = 0 A		620	700	830	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Not subject to production testing.

TYPICAL PERFORMANCE CURVES

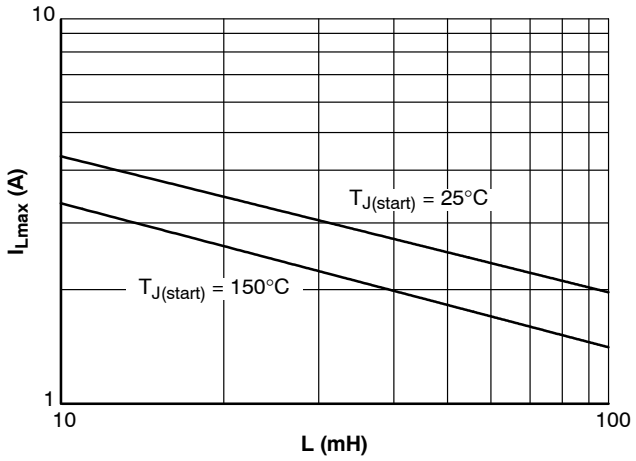


Figure 3. Single Pulse Maximum Switch−Off Current vs. Load Inductance

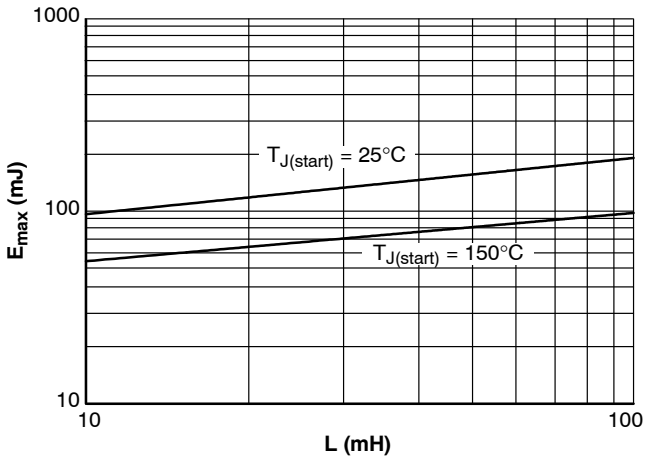


Figure 4. Single Pulse Maximum Switching Energy vs. Load Inductance

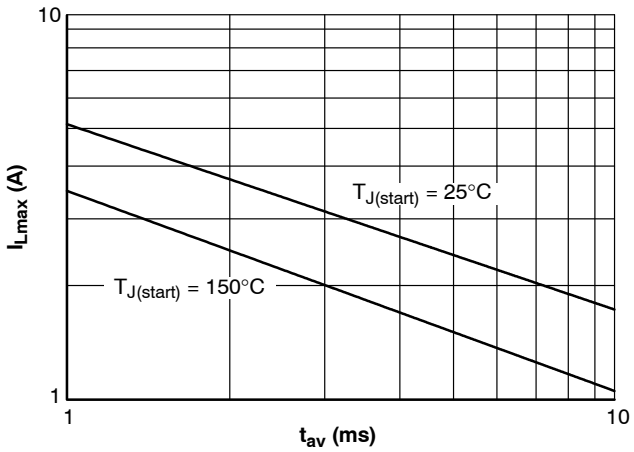


Figure 5. Single Pulse Maximum Inductive Switch−Off Current vs. Time in Avalanche

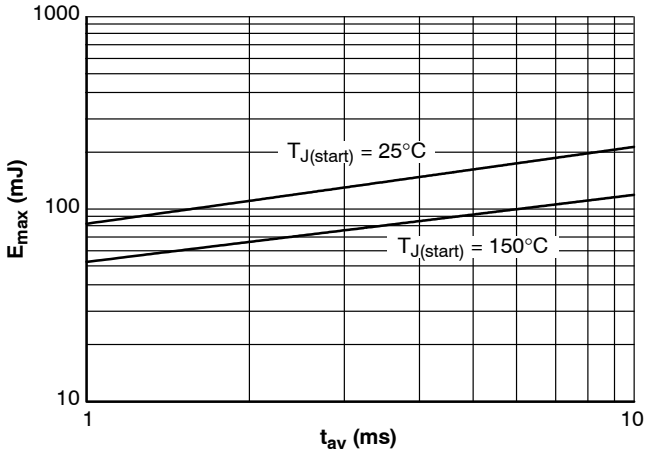


Figure 6. Single Pulse Maximum Inductive Switching Energy vs. Time in Avalanche

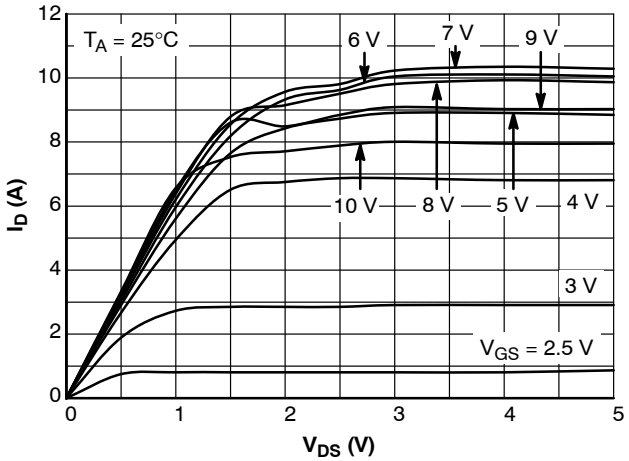


Figure 7. On−State Output Characteristics

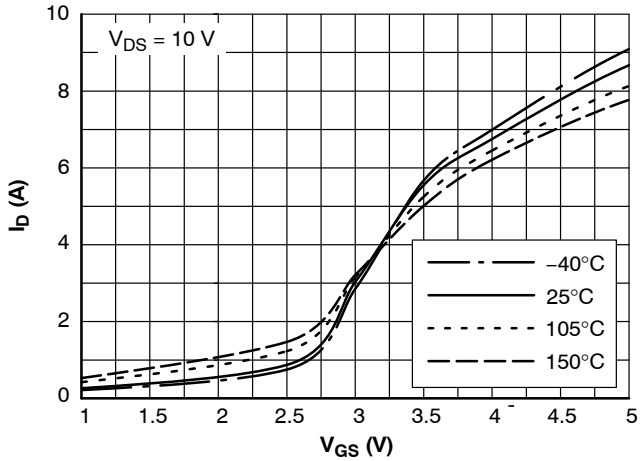


Figure 8. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

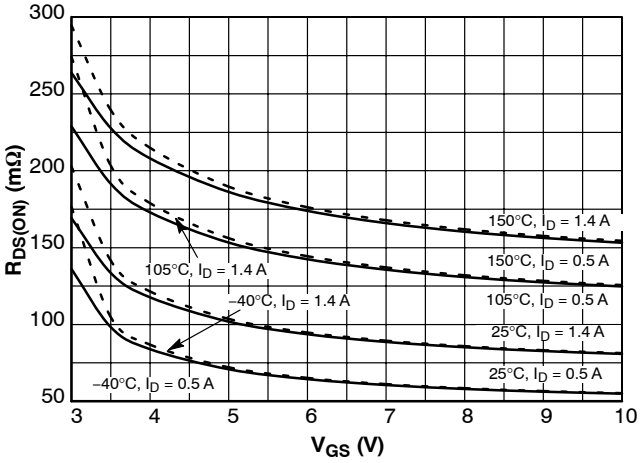


Figure 9. $R_{DS(ON)}$ vs. Gate−Source Voltage

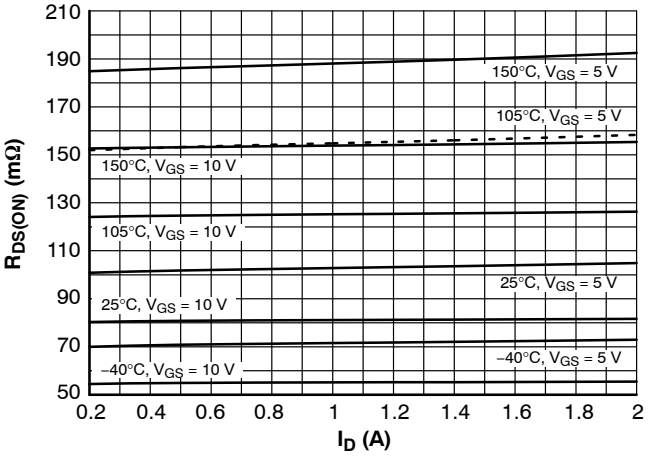


Figure 10. $R_{DS(ON)}$ vs. Drain Current

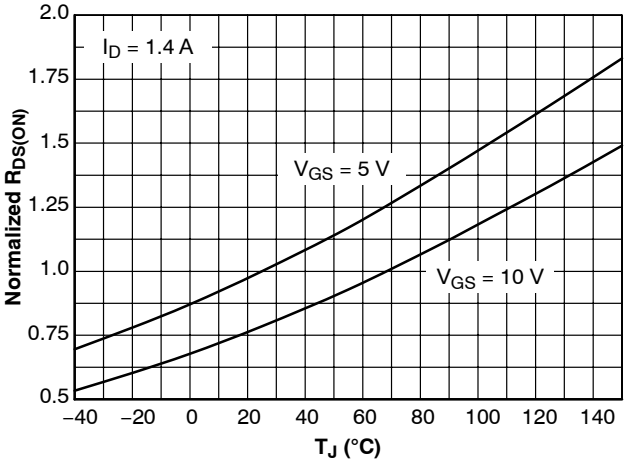


Figure 11. Normalized $R_{DS(ON)}$ vs. Temperature

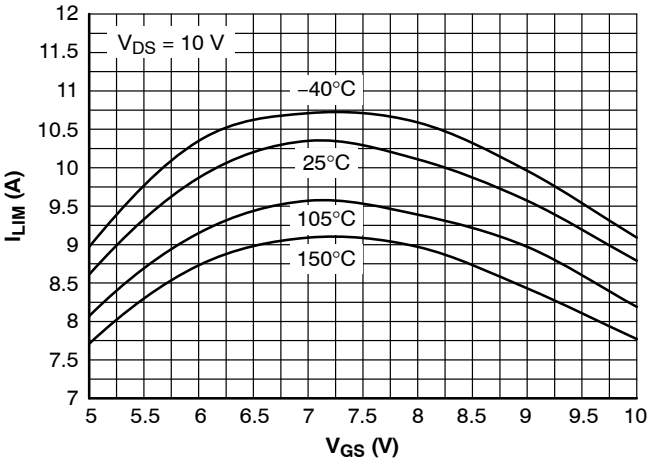


Figure 12. Current Limit vs. Gate−Source Voltage

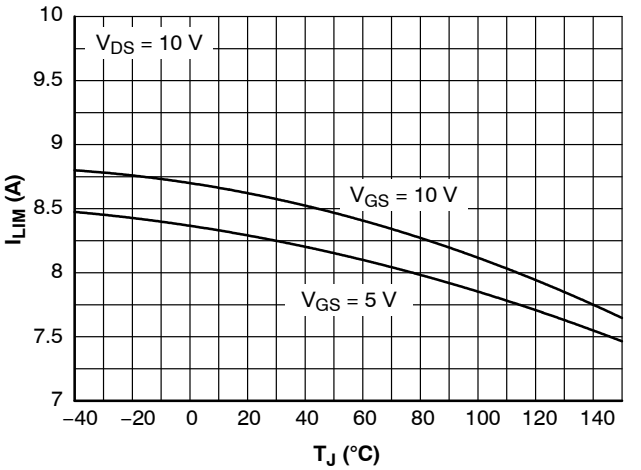


Figure 13. Current Limit vs. Junction Temperature

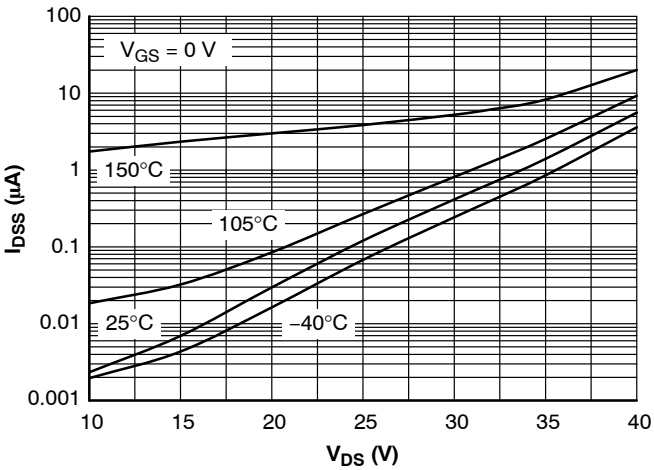


Figure 14. Drain−to−Source Leakage Current

TYPICAL PERFORMANCE CURVES

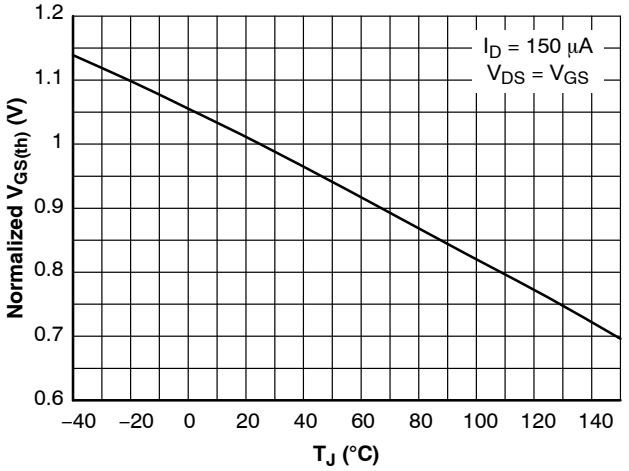


Figure 15. Normalized Threshold Voltage vs. Temperature

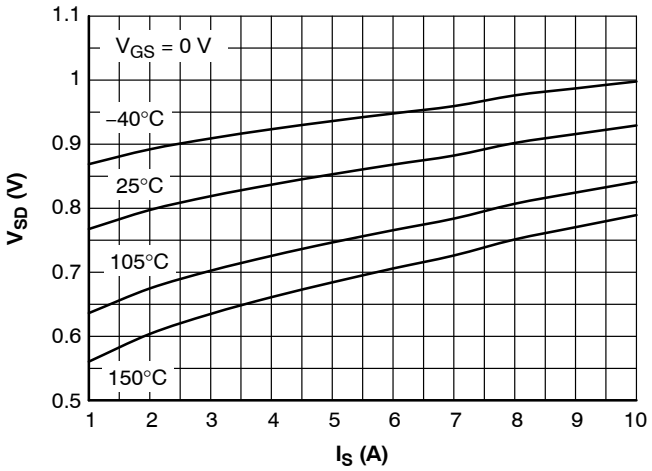


Figure 16. Source−Drain Diode Forward Characteristics

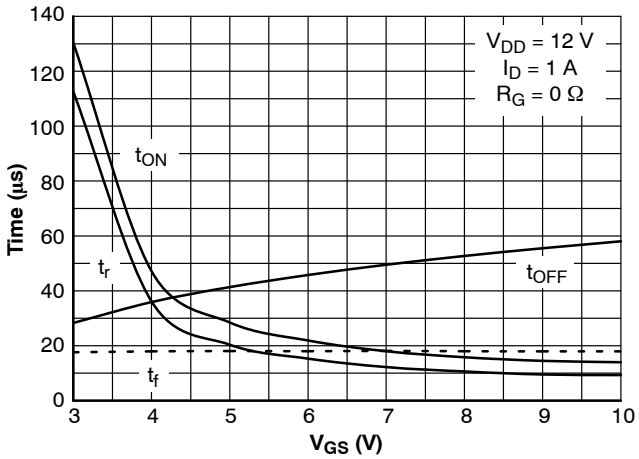


Figure 17. Resistive Load Switching Time vs. Gate−Source Voltage

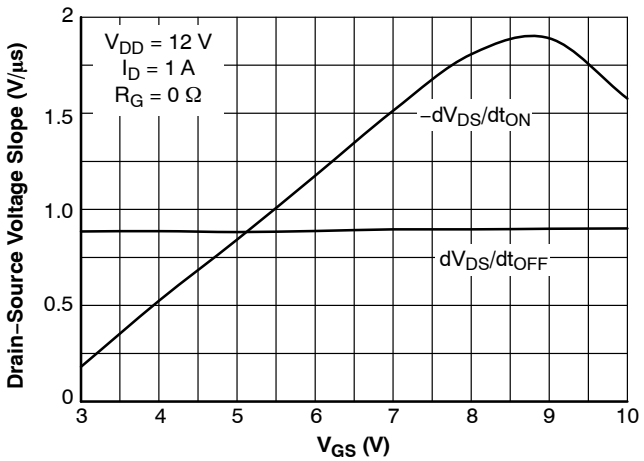


Figure 18. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage

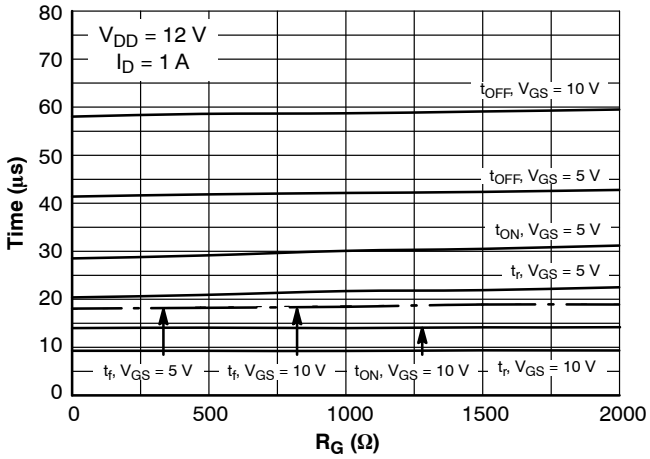


Figure 19. Resistive Load Switching Time vs. Gate Resistance

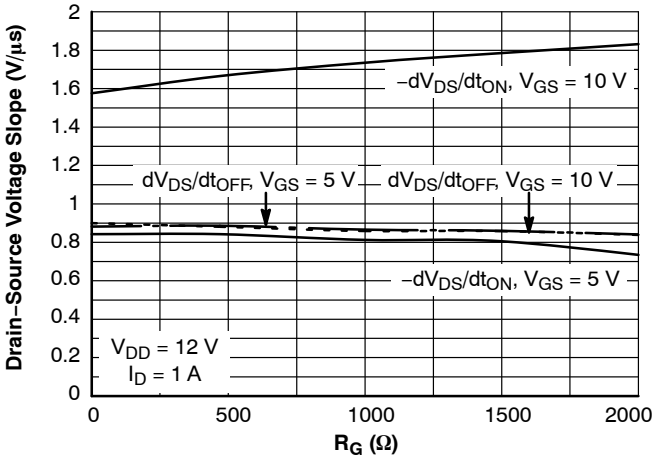


Figure 20. Resistive Load Switching Drain−Source Voltage Slope vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

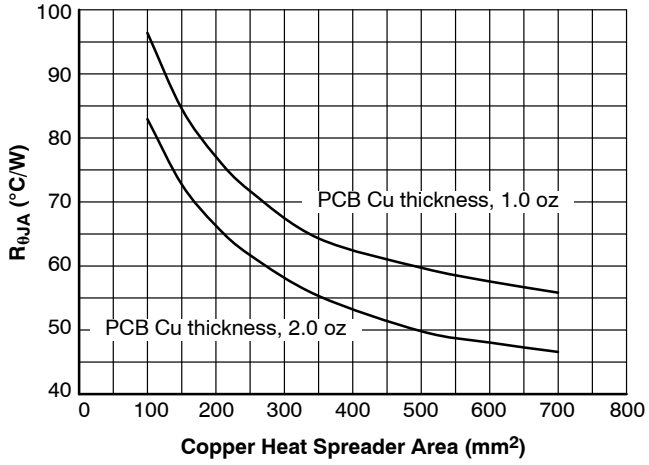


Figure 21. $R_{\theta JA}$ vs. Copper Area (SOT−223)

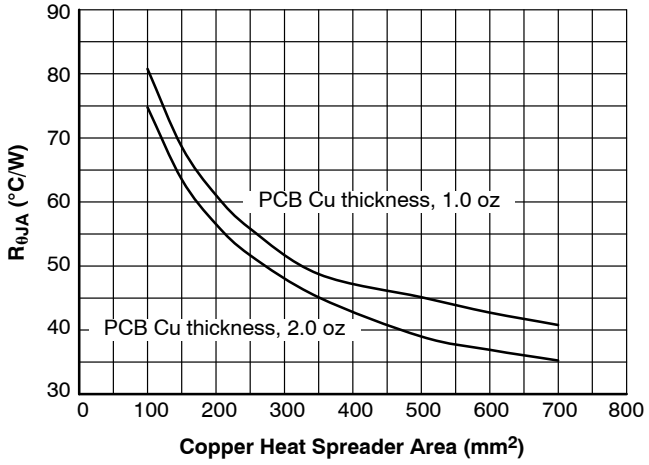


Figure 22. $R_{\theta JA}$ vs. Copper Area (DPAK)

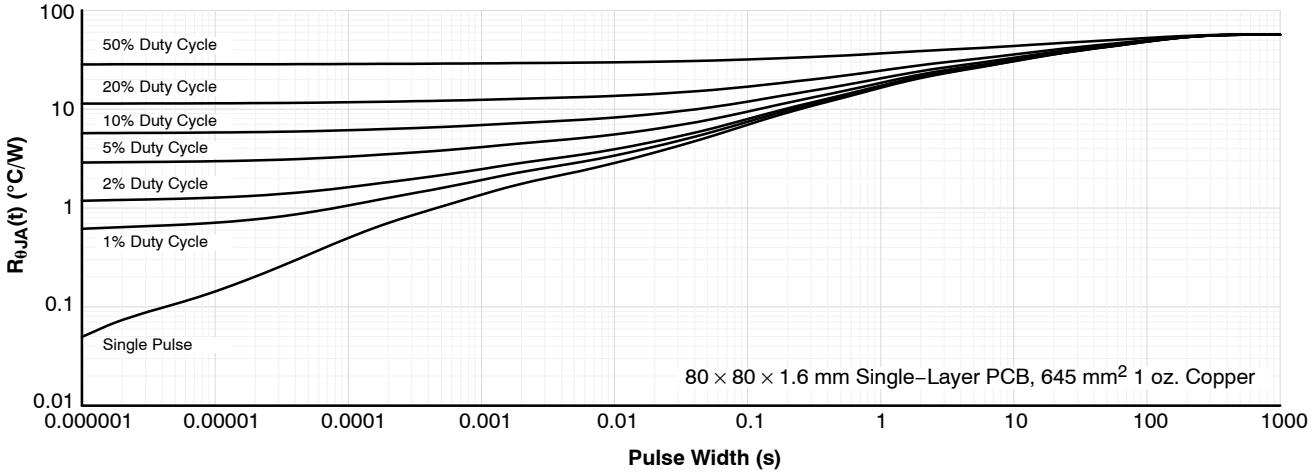


Figure 23. Transient Thermal Resistance (SOT−223)

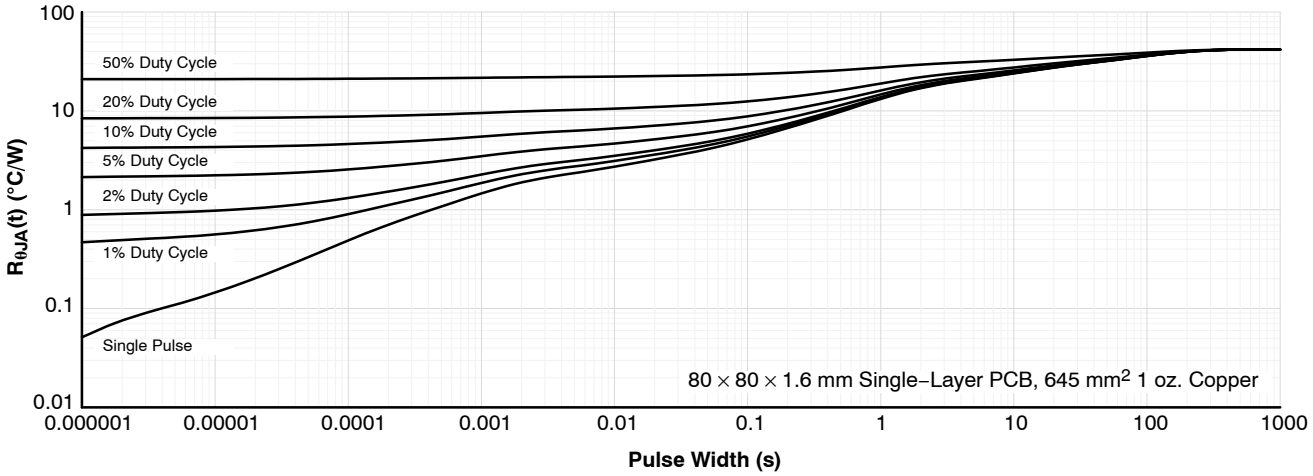


Figure 24. Transient Thermal Resistance (DPAK)

APPLICATION INFORMATION

Circuit Protection Features

The NCV8415 has three main protections. Current Limit, Thermal Shutdown and Delta Thermal Shutdown. These protections establish robustness of the NCV8415.

Current Limit and Short Circuit Protection

The NCV8415 has current sense element. In the event that the drain current reaches designed current limit level, integrated Current Limit protection establishes its constant level.

Delta Thermal Shutdown

Delta Thermal Shutdown (DTSD) Protection increases higher reliability of the NCV8415. DTSD consist of two independent temperature sensors – cold and hot sensors. The NCV8415 establishes a slow junction temperature rise by sensing the difference between the hot and cold sensors. ON/OFF output cycling is designed with hysteresis that results in a controlled saw tooth temperature profile (Figure 26). The die temperature slowly rises (DTSD) until the absolute temperature shutdown (TSD) is reached around 175°C.

Thermal Shutdown with Automatic Restart

Internal Thermal Shutdown (TSD) circuitry is provided to protect the NCV8415 in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the NCV8415 turns off. This feature is provided to prevent failures from accidental overheating.

EMC Performance

To improve the EMC performance/robustness, connect a small ceramic capacitor to the drain pin as close to the device as possible according to Figure 25.

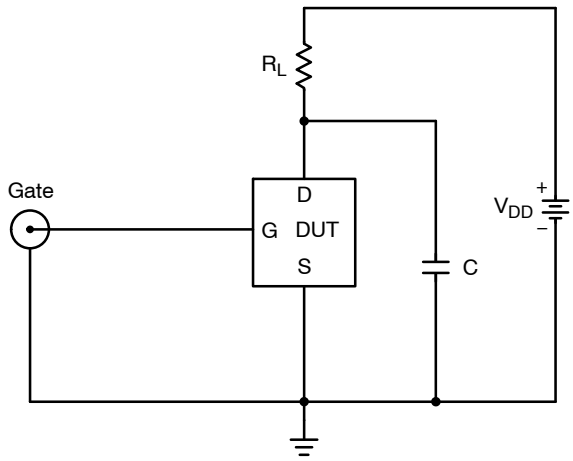


Figure 25. EMC Capacitor Placement

TEST CIRCUITS AND WAVEFORMS

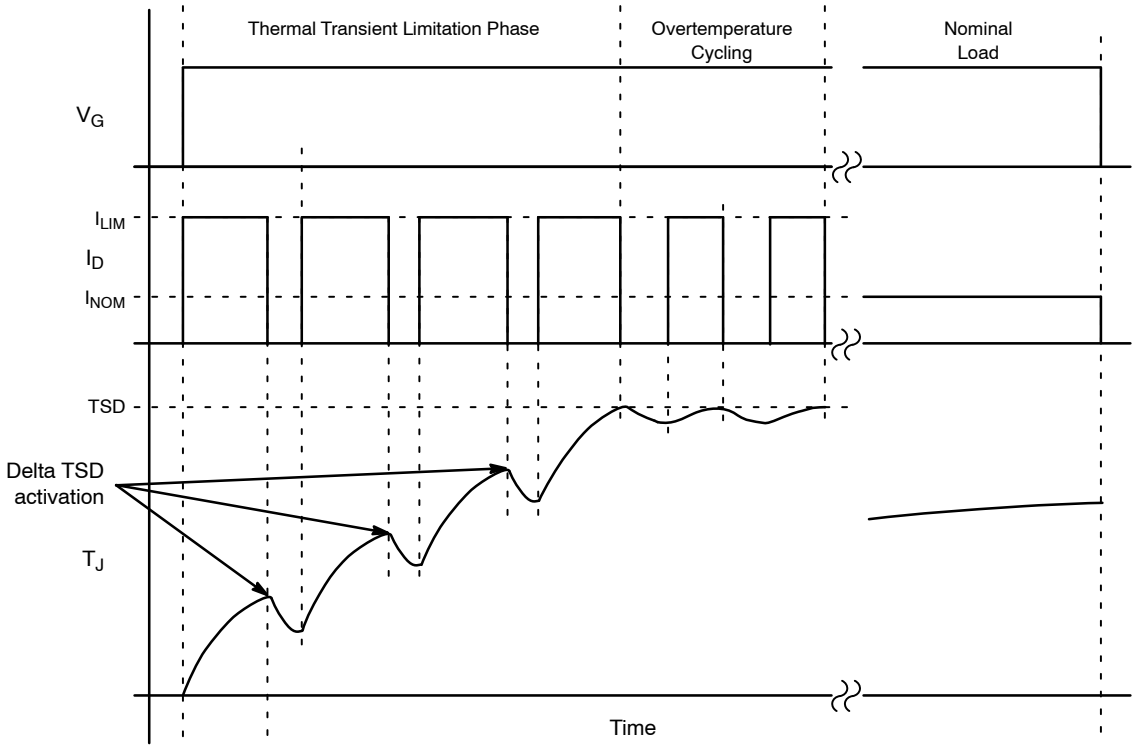


Figure 26. Overload Protection Behavior

TEST CIRCUITS AND WAVEFORMS

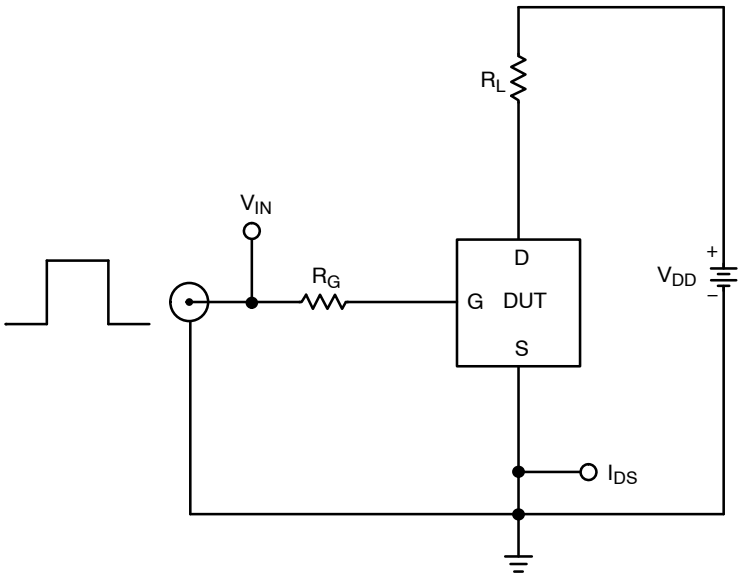


Figure 27. Resistive Load Switching Test Circuit

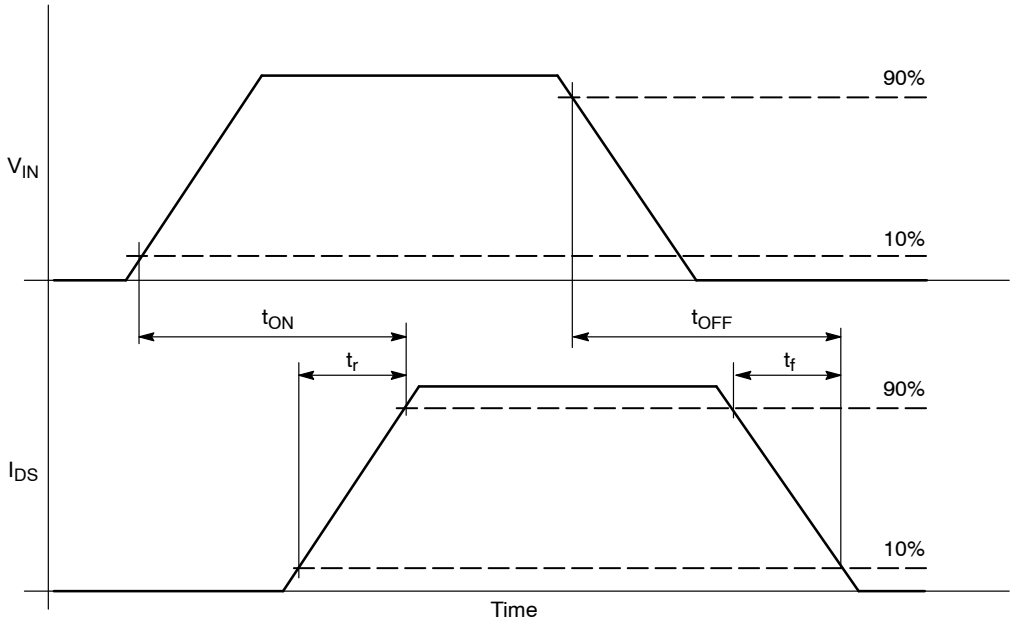


Figure 28. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

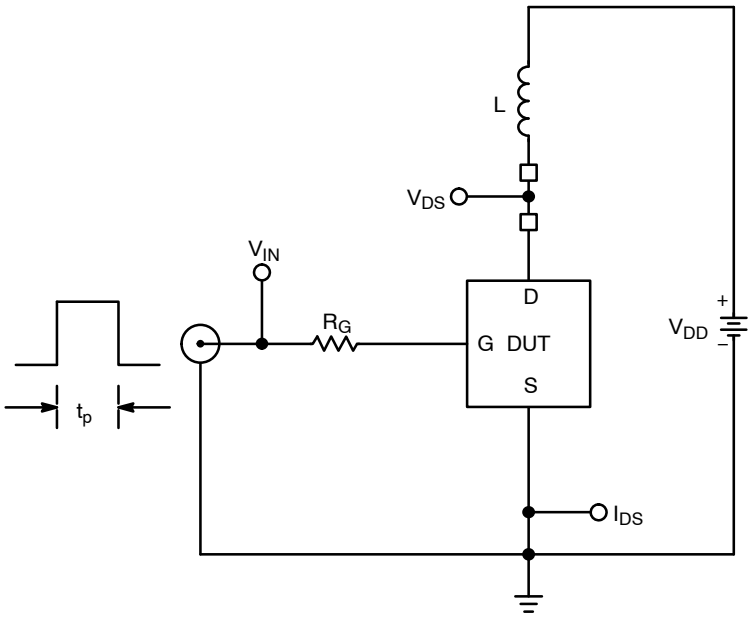


Figure 29. Inductive Load Switching Test Circuit

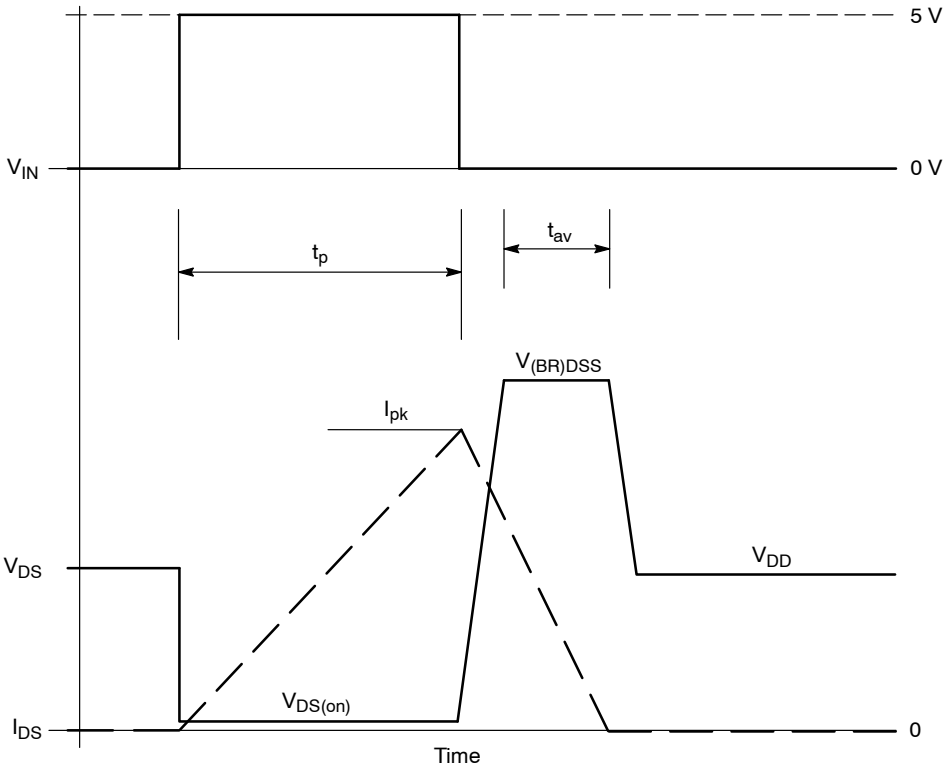
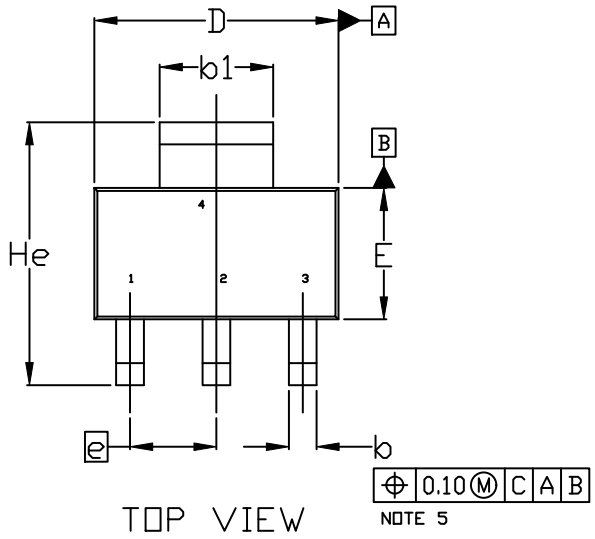


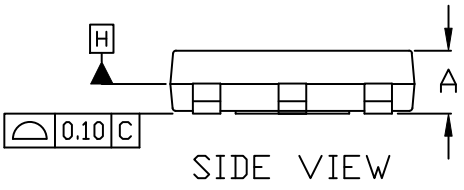
Figure 30. Inductive Load Switching Waveforms

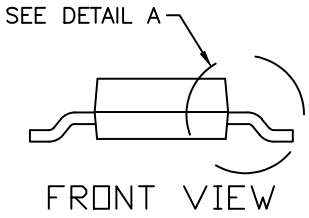
SCALE 1:1

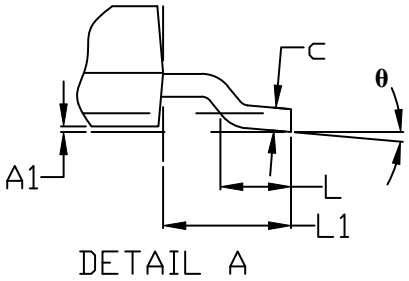
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



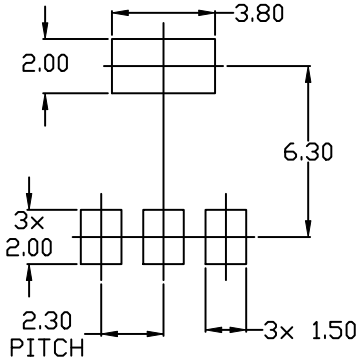






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

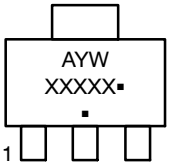
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

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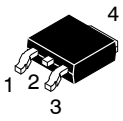
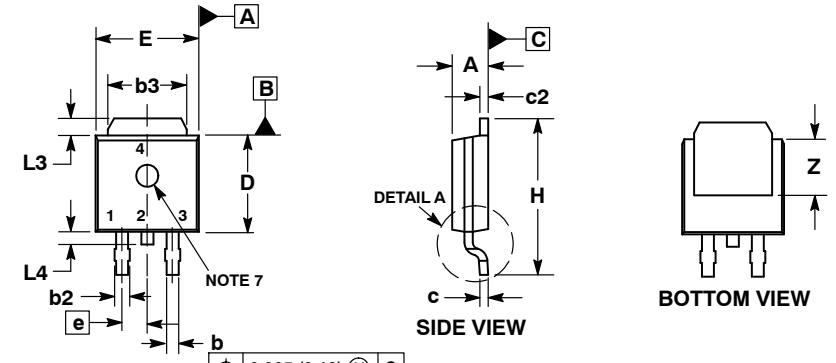
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

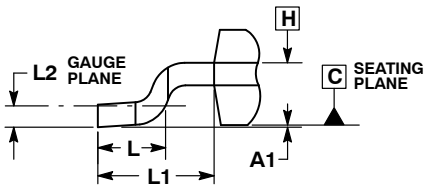
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

DATE 21 JUL 2015

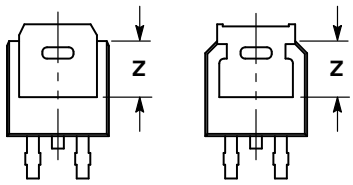


SCALE 1:1





DETAIL A
ROTATED 90° CW



BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

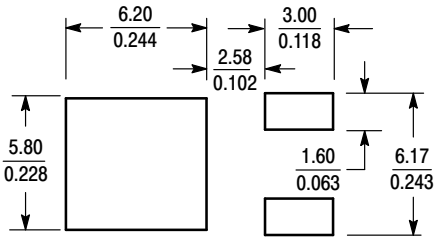
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

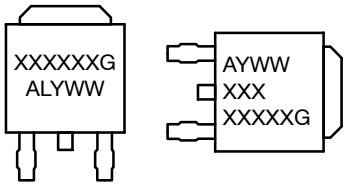
SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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